IN THE UNITED STATES
PATENT AND TRADEMARK OFFICE

Appl. No. : **10/029,829**

Confirmation No. : **5503**

Applicant(s) : **ZHONG et al.**

Filed : **27 Dec 2001**

TC/A.U. : **2621**

Examiner : **LEE, Y. Young**

Atty. Docket : **US-010719**

Title: **DYNAMIC CONTROL IN COMPLEXITY-CONSTRAINED DATA COMPRESSION**

Mail Stop: **APPEAL BRIEF - PATENTS**
Commissioner for Patents
Alexandria, VA 22313-1450

APPEAL UNDER 37 CFR 41.37

Sir:

This is an appeal from the decision of the Examiner dated 15 November 2006, rejecting claims 1-21 of the subject application, the claims having been at least twice rejected.

This paper includes (each beginning on a separate sheet):

1. **Appeal Brief, with appendices.**

APPEAL BRIEF

I. REAL PARTY IN INTEREST

The above-identified application is assigned, in its entirety, to **Koninklijke Philips Electronics N. V.**

II. RELATED APPEALS AND INTERFERENCES

Appellant is not aware of any co-pending appeal or interference that will directly affect, or be directly affected by, or have any bearing on, the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

Claims 1-21 are pending in the application.

Claims 1-6, 8-15, and 17-21 stand rejected by the Examiner under 35 U.S.C. 102(b).

Claims 7 and 16 stand rejected by the Examiner under 35 U.S.C. 103(a).

These rejected claims are the subject of this appeal.

IV. STATUS OF AMENDMENTS

No amendments were filed subsequent to the rejection in the Office Action dated 15 November 2006.

V. SUMMARY OF CLAIMED SUBJECT MATTER

According to one embodiment, the invention addresses control of an encoding process based on a fullness measure of an input buffer (Applicants' specification, page 3, lines 6-11), and has particular application for encoding video data into an MPEG format using a performance-limited encoder, such as a software-based MPEG encoder (page 2, lines 12-17). The encoder is designed to keep up with the delivery rate of the incoming data (FIG. 4); if the input buffer becomes full, the encoding complexity is decreased (140-150 of FIG. 4); when sufficient buffer space becomes available, the encoding complexity can be increased (160-170 of FIG. 4; page 3,

lines 11-19).

As claimed in independent claim 1, one embodiment of the invention comprises a method for encoding a stream of data blocks using a scalable encoder, the method comprising:

receiving a stream of data blocks (page 3, line 7);

storing said received data blocks in an input buffer (14 of FIG. 1; page 3, line 8);

encoding (16 of FIG. 1; 110 of FIG. 4) a first sequence of said stored data blocks from said input buffer to produce a first encoded data block (page 3, lines 8-9);

monitoring (120 of FIG. 4) the fullness level of said input buffer for comparison with a predetermined threshold range to yield an outcome of said comparison (page 3, lines 9-10); and

adjusting (150, 170 of FIG. 4) the complexity of said encoder based on said outcome (page 3, lines 10-11).

As claimed in independent claim 9, one embodiment of the invention comprises a method for encoding a stream of data blocks using a scalable encoder, comprising:

temporarily storing the stream of said data blocks in an input buffer (14 of FIG. 1; page 4, lines 4-5);

retrieving a first sequence of said stored data blocks from said input buffer (page 4, line 5);

encoding (16 of FIG. 1; 110 of FIG. 4) the first sequence of said stored data blocks from said input buffer to produce a first encoded data block (page 4, lines 6-7);

monitoring (120 of FIG. 4) the fullness level of said input buffer (page 4, line 7);

comparing (130 of FIG. 4) the fullness level of said input buffer to a predetermined threshold range (page 4, lines 7-8);

increasing (160-170 of FIG. 4) the complexity of said encoder when the fullness level of said input buffer is below a lower level of said predetermined

threshold range (page 4, lines 8-10); and

decreasing (140-150 of FIG. 4) the complexity of said encoder when the fullness level of said input buffer is above an upper level of said predetermined threshold range (page 4, lines 10-11).

As claimed in independent claim 17, one embodiment of the invention comprises an encoding system (FIG. 1) for encoding a stream of datablocks, comprising:

an analog-to-digital converter (12) for converting analog signals from a plurality of sources into digital signals (page 4, lines 20-21);

an input buffer (14) for receiving said converted digital signals at a predefined rate (page 4, lines 21-22);

a memory (20) for storing a predetermined encoding table (page 4, line 22 – page 5, line 1);

an encoder (16) for encoding the stream of data blocks stored in said input buffer (page 5, line 1);

a management module (18), operatively coupled to said input buffer, said encoder, and said memory (page 5, lines 1-2),

wherein said management module is operable to (FIG. 4): (a) receive the stream of said data blocks; (b) store said received data blocks in said input buffer; (c) cause to encode (110) a first sequence of said stored data blocks from said input buffer to produce a first encoded data block; (d) monitor (120) the fullness level of said input buffer for comparison with a predetermined threshold range; (e) cause to adjust (150, 170) the complexity of said encoder based on only said comparison outcome of said input buffer and said predetermined encoding table, said configuration table using a plurality of complexities and encoding options; and, (f) cause to encode (150-110, 170-110) a second data block at said adjusted complexity to produce a second encoded data block (page 5, lines 2-9).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1-6, 8-15, and 17-21 stand rejected under 35 U.S.C. 102(b) over Iwahashi et al. (USP 5,197,087, hereinafter Iwahashi).

Claims 7 and 16 stand rejected under 35 U.S.C. 103(a) over Iwahashi and Ishiyama (USPA 2001/0008544).

VII. ARGUMENT

Claims 1-6, 8-15, and 17-21 stand rejected under 35 U.S.C. 102(b) over Iwahashi

MPEP 2131 states:

> "A claim is anticipated only if ***each and every element*** as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). "The ***identical invention*** must be shown in as ***complete detail*** as is contained in the ... claim." *Richardson v. Suzuki Motor Co*., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Claims 1-6 and 8

Claim 1, upon which claims 2-8 depend, claims a method for encoding a stream of data blocks that includes storing a stream of received data blocks in an input buffer, monitoring the fullness level of the input buffer for comparison with a predetermined threshold range, and adjusting the complexity of an encoder based on the outcome of the comparison.

Iwahashi does not teach adjusting the complexity of an encoder based on a comparison of a fullness level of an input buffer and a predetermined threshold. The Office action asserts that Iwahashi teaches monitoring the fullness level of an input buffer for comparison with a predetermined threshold value, but fails to identify where Iwahashi provides this teaching.

Iwahashi teaches loading two halves of a data block into two buffers 11, 12, and adjusting an encoder 17 based on a comparison of the energy in the data values of each buffer 11 and 12 (Iwahashi, column 3, line 60 - column 4, line 27). That is, both buffers 11 and 12 include L/2 data values, where L is equal to the block size. The magnitude of the fluctuations in stored data values is used as a measure of the

energy in the signal, and this energy value is compared to a threshold to control the input to encoder 17 (Iwahashi, column 4, lines 42-52).

Because Iwahashi fails to teach adjusting the complexity of an encoder based on a comparison of a fullness level of an input buffer and a predetermined threshold, as specifically claimed in claim 1, the applicants respectfully maintain that the rejection of claims 1-6 and 8 under 35 U.S.C. 102(b) over Iwahashi is unfounded, per MPEP 2131.

Claims 9-15

Claim 9, upon which claims 10-16 depend, claims a method that includes storing a stream of the data blocks in an input buffer, increasing the complexity of an encoder when the fullness level of the input buffer is below a lower level of the predetermined threshold range, and decreasing the complexity of the encoder when the fullness level of the input buffer is above an upper level of the predetermined threshold range.

As noted above, Iwahashi fails to teach controlling the complexity of an encoder based on a fullness level of an input buffer. Iwahashi controls the input of an encoder based on the energy level contained in the data that is stored in a buffer.

Because Iwahashi fails to teach increasing or decreasing the complexity of an encoder when the fullness level of the input buffer is below a lower level or above a higher level of a predetermined threshold range, as specifically claimed in claim 9, the applicants respectfully maintain that the rejection of claims 9-15 under 35 U.S.C. 102(b) over Iwahashi is unfounded, per MPEP 2131.

Claims 17-21

Claim 17, upon which claims 18-21 depend, claims an encoding system that includes a management module that is operable to: (a) receive a stream of data blocks; (b) store the received data blocks in an input buffer; (c) cause to encode a first sequence of the stored data blocks from the input buffer; (d) monitor the fullness level of the input buffer for comparison with a predetermined threshold range; (e)

cause to adjust the complexity of an encoder based on the comparison outcome; and, (f) cause to encode a second data block at the adjusted complexity to produce a second encoded data block.

As noted above, Iwahashi fails to teach monitoring the fullness level of the input buffer for comparison with a predetermined threshold range; and fails to teach adjusting the complexity of an encoder based on the comparison outcome.

Because Iwahashi fails to teach each of the elements of claim 17, the applicants respectfully maintain that the rejection of claims 17-21 under 35 U.S.C. 102(b) over Iwahashi is unfounded, per MPEP 2131.

Claims 7 and 16 stand rejected under 35 U.S.C. 103(a) over Iwahashi and Ishiyama

MPEP 2142 states:

> "To establish a *prima facie* case of obviousness ... the prior art reference (or references when combined) ***must teach or suggest all the claim limitations***... If the examiner does not produce a *prima facie* case, the applicant is under no obligation to submit evidence of nonobviousness."

Claim 7

Claim 7 is dependent upon claim 1; in this rejection, the Office action relies upon Iwahashi for teaching the elements of claim 1. As noted above, Iwahashi fails to teach the elements of claim 1. Accordingly, the applicants respectfully maintain that the rejection of claim 7 under 35 U.S.C. 103(a) that relies upon Iwahashi for teaching the elements of claim 1 is unfounded, per MPEP 2142.

Claim 16

Claim 16 is dependent upon claim 9; in this rejection, the Office action relies upon Iwahashi for teaching the elements of claim 9. As noted above, Iwahashi fails to teach the elements of claim 9. Accordingly, the applicants respectfully maintain that the rejection of claim 16 under 35 U.S.C. 103(a) that relies upon Iwahashi for teaching the elements of claim 9 is unfounded, per MPEP 2142.

CONCLUSIONS

Because Iwahashi fails to teach controlling the complexity of an encoder based on the fullness of an input buffer, the applicants respectfully request that the Examiner's rejection of claims 1-6, 8-15, and 17-21 under 35 U.S.C. 102(b) over Iwahashi, and claims 7 and 16 under 35 U.S.C. 103(a) over Iwahashi and Ishiyama be reversed by the Board, and the claims be allowed to pass to issue.

Respectfully submitted,

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CLAIMS APPENDIX

1. A method for encoding a stream of data blocks using a scalable encoder, the method comprising:

receiving a stream of data blocks;

storing said received data blocks in an input buffer;

encoding a first sequence of said stored data blocks from said input buffer to produce a first encoded data block;

monitoring the fullness level of said input buffer for comparison with a predetermined threshold range to yield an outcome of said comparison; and

adjusting the complexity of said encoder based on said outcome.

2. The method of claim 1, wherein the step of adjusting the complexity of said encoder based on said comparison outcome comprises:

decreasing the complexity of said encoder when the fullness level of said input buffer exceeds an upper limit of said threshold range; and,

encoding a second data block at the decreased complexity to produce a second encoded data block.

3. The method of claim 2, wherein decreasing the complexity of said encoder is performed according to a predetermined encoding configuration table.

4. The method of claim 1, wherein adjusting the complexity comprises:

increasing the complexity of said encoder when the fullness level of said input buffer is below a lower level of said predetermined threshold range; and,

encoding a second data block at the increased complexity to produce a second encoded data block.

5. The method of claim 4, wherein increasing the complexity of said encoder is performed according to a predetermined encoding configuration table.

6. The method of claim 1, wherein adjusting the complexity comprises maintaining the complexity of said encoder when the fullness level of said input buffer falls within said predetermined threshold range.

7. The method of claim 1, further comprising storing said first encoded data block in a memory medium for subsequent retrieval.

8. The method of claim 1, wherein the stream of data blocks comprises a stream of video frames.

9. A method for encoding a stream of data blocks using a scalable encoder, comprising:

temporarily storing the stream of said data blocks in an input buffer;

retrieving a first sequence of said stored data blocks from said input buffer;

encoding the first sequence of said stored data blocks from said input buffer to produce a first encoded data block;

monitoring the fullness level of said input buffer;

comparing the fullness level of said input buffer to a predetermined threshold range;

increasing the complexity of said encoder when the fullness level of said input buffer is below a lower level of said predetermined threshold range; and

decreasing the complexity of said encoder when the fullness level of said input buffer is above an upper level of said predetermined threshold range.

10. The method of claim 9, further comprising encoding a second data block at the increased complexity to produce a second encoded data block.

11. The method of claim 9, wherein increasing and decreasing the complexity of said encoder are performed according to a predetermined encoding configuration table.

12. The method of claim 9, further comprising encoding a second data block at the decreased complexity to produce a second encoded data block.

13. The method of claim 9, further comprising maintaining the complexity of said encoder when the fullness level of said input buffer falls within said predetermined threshold range.

14. The method of claim 9, further comprising storing said first encoded data block in a memory medium for subsequent retrieval.

15. The method of claim 9, wherein the stream of data blocks comprises a stream of video frames.

16. The method of claim 9, wherein the fullness level of said input buffer is determined based on an input rate of the stream of said data blocks and processing feedback information from said encoder after producing said first encoded data block.

17. An encoding system for encoding a stream of datablocks, comprising:

an analog-to-digital converter for converting analog signals from a plurality of sources into digital signals;

an input buffer for receiving said converted digital signals at a predefined rate;

a memory for storing a predetermined encoding table;

an encoder for encoding the stream of data blocks stored in said input buffer;

a management module, operatively coupled to said input buffer, said encoder, and said memory,

wherein said management module is operable to: (a) receive the stream of said data blocks; (b) store said received data blocks in said input buffer; (c) cause to encode a first sequence of said stored data blocks from said input buffer to produce a first encoded data block; (d) monitor the fullness level of said input buffer for comparison with a predetermined threshold range; (e) cause to adjust the complexity

of said encoder based on only said comparison outcome of said input buffer and said predetermined encoding table, said configuration table using a plurality of complexities and encoding options; and, (f) cause to encode a second data block at said adjusted complexity to produce a second encoded data block.

18. The system of claim 17, wherein said management module is further operable to decrease the complexity of said encoder when the fullness level of said input buffer exceeds an upper limit of said threshold range.

19. The system of claim 17, wherein said management module is further operable to increase the complexity of said encoder when the fullness level of said input buffer is below a lower level of said predetermined threshold range.

20. The system of claim 17, wherein said management module is further operable to maintain the complexity of said encoder when the fullness level of said input buffer falls within said predetermined threshold range.

21. The system of claim 17, wherein the stream of data blocks comprises a stream of video frames.

EVIDENCE APPENDIX

No evidence has been submitted that is relied upon by the appellant in this appeal.

RELATED PROCEEDINGS APPENDIX

Appellant is not aware of any co-pending appeal or interference which will directly affect or be directly affected by or have any bearing on the Board's decision in the pending appeal.